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PATENT

Applicant: Lap Wai Chow, et al.

) Group Art No.: 2812

Application No: 09/768,911

) Examiner: David A. Zarneke

Filed: January 24, 2001

) **RESPONSE**

For: "INTEGRATED CIRCUITS PROTECTED..." Date: October 25, 2001

) Our Ref: B-3962 618027-2/RPB

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

This paper is filed in Response to the Official Action dated September 25, 2001. Please add the following new claims to this Application:

17. A semiconducting device adapted to prevent and/or to thwart reverse engineering, including:

(a) an insulating layer disposed on a semiconductor substrate;

(b) a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said insulating layer; and

(c) a via defined by said insulating layer, said via having a first end and a second end,

wherein one end of said via is connected to one of said first metal layer and said second metal layer and wherein another end of said via terminates prior to reaching at least one of said first metal layer and said second metal layer.

18. A method for making a semiconductor device for preventing and/or thwarting reverse engineering thereof, comprising steps of:

(a) disposing an insulating layer on a semiconductor substrate;

(b) defining a first electrically conductive layer and a second electrically conductive layer so that said first electrically conductive layer and said second electrically conductive layer are separated by said insulating layer; and